Amendments to the Claims:

Claim 1 (Currently Amended): A circuit for current regulation, comprising:

a regulation circuit coupled to a power supply and configured to generate a regulated current to a load;

a mode circuit having an input coupled to a control signal and an output configured to generate a mode signal relating to an open mode and a linear mode associated with the regulation circuit;

a comparator having an input coupled to a signal relating to a voltage associated with the regulation circuit, an input coupled to the mode signal and configured to compare the mode signal and the signal relating to the voltage[~~,~~], wherein the signal relating to the voltage is used to indicate when the regulation circuit is in a saturation overload condition;

a switch circuit coupling an output of the comparator to a linear mode control node when the circuit is operating in the linear mode and to an open mode control node when the circuit is operating in the open mode; and ~~a~~

a control circuit coupled to the mode circuit and configured to generate a control signal used in controlling the mode circuit.

Claim 2 (original): The circuit of Claim 1, wherein the regulation circuit is a transistor that operates one of the linear control mode and the open mode.

Claim 3 (original): The circuit of Claim 1, wherein the mode circuit further comprises a multiplexer and a resistor ladder that is coupled to a reference signal.

Claim 4 (original): The circuit of Claim 3, wherein the multiplexer is coupled to the control signal and arranged to select a tap point associated with the resistor ladder.

Claim 5 (original): The circuit of Claim 2, wherein the transistor is a PNP transistor.

Claim 6 (original): The circuit of Claim 1, wherein the switch circuit is configured to switch from the open mode to the linear control mode when the regulation circuit is in a overloaded state.

Claim 7 (original): The circuit of Claim 6, wherein the switch circuit is configured to switch back to the open mode.

Claim 8 (original): The circuit of Claim 4, wherein the control generates the control signal such that the multiplexer selects different tap points while the circuit operates in the linear mode.

Claim 9 (Currently Amended): An apparatus for current regulation, comprising:

a transistor configured to operate in a linear control mode and an open mode and that has an emitter coupled to an emitter node and a collector coupled to a collector node;

a ~~second~~ node that is coupled to a signal that is proportional to a voltage across the transistor configured to operate in the linear control mode and the open mode;

a comparator having an input coupled to a mode signal, an input coupled to the ~~second~~ node, and arranged to compare the inputs and output an output signal, wherein the input coupled to the node is used to indicate when the transistor is in a saturation overload condition;;

a switch circuit coupled to the output signal and configured to couple the output signal to a linear mode node when the circuit is operating in the linear control mode; and to the open mode node when the circuit is operating in the open mode;

a control circuit coupled to the linear mode node and to the open mode node and configured to generate a control signal; and

a mode circuit coupled to the control signal and configured to output the mode signal in response to the control signal.

Claim 10 (original): The apparatus of Claim 9, wherein the transistor is a PNP transistor.

Claim 11 (original): The apparatus of Claim 10, wherein the mode circuit further comprises a multiplexer coupled to the control signal and a resistor ladder that is coupled to the multiplexer.

Claim 12 (original): The apparatus of Claim 10, wherein the mode circuit outputs a constant signal when the circuit is in the open mode.

Claim 13 (original): The apparatus of Claim 11, wherein the multiplexer selects tap points in the resistor ladder when the circuit is in the linear mode.

Claim 14 (Currently Amended): The apparatus of Claim 9, further comprising an amplifier having an input coupled to ~~an~~ the emitter node, an input coupled to ~~a~~ the collector node and an output coupled to a gate of a second transistor; wherein ~~and a~~ the second transistor is coupled to the emitter node and the ~~second~~ node;

Claim 15 (original): A method for current regulation of a circuit, comprising:
comparing a signal to an overload signal when in an open mode;
determining when a regulation circuit is overloaded;
changing to a linear mode when overloaded; and when the circuit is in the linear mode:
adjusting a multiplexer to select a tap point in a resistor ladder; and
comparing the signal to a signal associated with the selected tap point using the same comparator that compared the signal to the overload signal.

Claim 16 (original): The method of Claim 15, further comprising switching back to the open mode.

Claim 17 (original): An apparatus for current regulation, comprising:
means for comparing a signal to an overload signal when in an open mode;
means for determining when a regulation circuit is overloaded when the circuit is operating in the open mode;

means for changing to a linear mode when the regulation circuit is overloaded; and when the circuit is operating in the linear mode:

means for adjusting a multiplexer to select a tap point in a resistor ladder; and

means for comparing the signal to a signal associated with the selected tap point using the same comparator that compared the signal to the overload signal.

Claim 18 (original): The apparatus of Claim 17, further comprising means for switching the circuit back to the open mode.